

**WHAT IS CLAIMED IS:**

1. A time-slot interchange circuit comprising:

5 a plurality of input data streams;

a plurality of m-stage shift registers, such that each shift register corresponds to one of the input data streams and the bits within each input data stream are sequentially clocked through the corresponding shift register; and

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a multiplexer adapted to select a bit from the m<sup>th</sup> stage of any of the shift registers and insert it into an output data stream.

2. The time-slot interchange circuit as recited in claim 1, wherein the input data  
15 streams comprise signals that have been time-division multiplexed (TDM) and wherein the bits within each input data stream represent TDM voice data occupying time-slots in a frame of data, as typically used for telephone communication.

3. The time-slot interchange circuit as recited in claim 2, further comprising a  
20 plurality of multiplexers and a corresponding plurality of output data streams, said output data streams comprising TDM signals, sharing a common clock and frame-sync timing.

4. The time-slot interchange circuit as recited in claim 1, wherein  $m = 2$ .

25 5. A method for redistributing bits arriving in an input data stream to a corresponding output data stream, comprising:

receiving a first sequence of data bits in a first input data stream;

30 receiving a second sequence of data bits in a second input data stream;

storing a first subsequence of the first sequence;

replacing a second subsequence of the second sequence with the stored first subsequence; and

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transmitting the replaced second subsequence as an output data stream.

6. A method for redistributing the bits arriving in a plurality of input data streams to an output data stream, comprising:

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sequentially clocking the bits in each input data stream through a corresponding m-stage shift register; and

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selecting a bit from the m<sup>th</sup> stage of any of the shift registers and inserting it into an output data stream.

7. The method as recited in claim 6, wherein any of said each input data stream comprises a time-division multiplexed signal, and the bits in each input data stream occupy time slots within a frame of data.

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8. The method as recited in claim 6, further comprising using a multiplexer to select the bit from the m<sup>th</sup> stage of any of the shift registers.

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9. The method as recited in claim 6, further comprising using a plurality of multiplexers to redistribute a plurality of bits arriving in a corresponding plurality of input data streams to a plurality of output data streams.

10. A telephony signaling circuit, comprising:

a comparison register adapted to store first signal bits contained within a first data sequence received over a voice channel; and

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a comparator adapted to compare the signal bits stored in the comparison register against second signal bits contained within a second data sequence received over the voice channel and, if the first signal bits differ from the second signal bits, to replace the first signal bits stored in the comparison register with the second signal bits and to notify a digital signal processor coupled to the comparator of the replacement.

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11. The telephony signaling circuit as recited in claim 10, further comprising a modification register adapted to store third signal bits, and a data modifier adapted to place the stored third signal bits into a third data sequence and to subsequently transmit the third data sequence over the voice channel.

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12. The telephony signaling circuit as recited in claim 11, further comprising multiple voice channels, such that each voice channel is adapted to receive a plurality of data sequences, each of which contains a unique combination of signal bits, and wherein one of a plurality of comparison registers, data comparators, modification registers and data modifiers is associated with each voice channel.

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13. The telephony signaling circuit as recited in claim 12, wherein in response to being notified by the data comparator of the replacement of the signal bits in the comparison register, the DSP changes, during use, the status of the respective voice channel.

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14. The telephony signaling circuit as recited in claim 12, wherein the DSP is configured to change the third signal bits stored in the modification register and cause the data modifier to place the changed third signal bits into a data sequence and to subsequently transmit the data sequence over the voice channel.

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15. The telephony signaling circuit as recited in claim 12, wherein the received and transmitted data sequences comprise time division multiplexed voice data, as typically used for telephone communication.

10 16. The telephony signaling circuit as recited in claim 12, further comprising a packet control processor (PCP) adapted to receive notification from the comparator of a change in the first signal bits stored in the comparison register, and to change third signal bits stored in the modification register.

15 17. The telephony signaling circuit as recited in claim 16, wherein receiving notification from the comparator comprises receiving a hardware interrupt issued by the comparator.

18. A method for detecting telephony signals, comprising:

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storing in a comparison register first signal bits contained within a first data sequence received over an input voice channel;

comparing the first signal bits against second signal bits contained in a second data sequence received over the input voice channel; and

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if the first signal bits differ from the second signal bits, replacing the first signal bits with the second signal bits.

19. The method as recited in claim 18, further comprising storing third signal bits in a modification register, using a data modifier to place the stored third signal bits into a third data sequence and subsequently transmitting the third data sequence over an output voice channel.

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20. The method as recited in claim 18, further comprising multiple input voice channels, such that each input voice channel is adapted to receive a plurality of data sequences, each of which contains a unique combination of signal bits, and wherein one of a plurality of comparison registers, data comparators, modification registers and data  
10 modifiers is associated with each input voice channel.

21. The method as recited in claim 18, further comprising multiple output voice channels, such that each output voice channel is adapted to transmit a data sequence containing a unique combination of signal bits, and wherein one of a plurality of  
15 modification registers and data modifiers is associated with each output voice channel.

22. The method as recited in claim 18, further comprising notifying a processor if the first signal bits differ from the second signal bits.

20 23. The method as recited in claim 19, further comprising the processor, upon being notified that the first signal bits differ from the second signal bits, changing the third signal bits stored in the modification register and causing the data modifier to place the changed third signal bits into the third data sequence, and subsequently transmit the third data sequence over the output voice channel.

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24. An integrated circuit voice processor, comprising:

a plurality of processors adapted to operate on digitized voice data;

5 a time-slot interchange circuit adapted to rearrange the time slots between frames of data received by the time-slot interchange circuit and frames of data sent from the time-slot interchange circuit to the processors;

10 a packet control processor adapted to convert the frames of data sent from the time-slot interchange circuit to a cell-based data format;

15 an asynchronous transfer mode (ATM) segmentation and reassembly (SAR) circuit adapted to segment the cell-based data format and to reconstruct the digitized voice data from the cell-based data format; and

a host interface adapted to communicate with an external processor.

25 The integrated circuit voice processor as recited in claim 22, wherein the plurality of processors, the time-slot interchange circuit, the packet control processor, the ATM SAR and the host interface are all integrated upon a single semiconductor substrate.